Sensitivity Analysis of Different Controller Parameters on the Stability of the Weak-grid-tied Interlinking VSC

Zhiwei Zeng, Jinbin Zhao, *Member, IEEE*, Sujie Zhang, Ling Mao, and Keqing Qu

***Abstract*—The stability problem arising from the DC-link voltage outer loop and current inner loop control in weak-grid-tied interlinking voltage-source converters (VSC) system has been extensively investigated. However, the different impacts on system stability caused by these controller parameters have not been well solved. A three-port hybrid AC/DC admittance-based model for VSC taking into account AC- and DC-side dynamics is developed for revealing the mechanism intuitively on the formation of the positive and negative feedback effects in the DC-link voltage control loop. Subsequently, the stability characteristics of the voltage outer loop and current inner loop controller parameters on VSC are analyzed. Compared to adjusting the voltage outer loop controller parameters which has significant effort on the dynamic regulation characteristics, it is more sensitive on system stability by the parameter change of the current inner loop controller. Theoretical results, along with experimental verification, are provided to validate the analysis.**

***Index Terms*—Weak-grid-tied interlinking VSC, admittance-based model, positive and negative feedback loop effects, stability.**

I. Introduction

Voltage-source converters (VSCs) are becoming increasingly prevalent in power system applications due to their efficient energy conversion and control [1]. For instance, VSCs are utilized to connect photovoltaic systems [2] and doubly-fed induction generators (DFIGs) in wind turbine applications to the grid [3].

In particular, in China, the utilization of VSC-HVDC systems, which employ VSCs at both terminals, has gained significant momentum. They are extensively employed for interconnecting AC grids and facilitating the integration of large-scale new energy. However, the substitution of traditional synchronous generators with power electronics converters reduces the strength of the grid, potentially leading to the occurrence of weak grids [4]–[6]. As an illustration, upon the commissioning of the back-to-back VSC-HVDC project (±420 kV/1250 MW) connecting Chongqing and Hubei province in China, a notable reduction in the minimum short circuit ratio on the Chongqing side is observed, reaching as low as 1.9 [7]. Weak grids can have a detrimental impact on the stability of the VSC system and pose significant challenges in terms of VSC control [8].

The stability of VSCs connected to weak grids has gained increasing attention, primarily owing to their complex dynamics resulting from multiple timescales. These dynamics arise from various control loops, including DC-link voltage outer control (DVC), grid synchronization, and current inner control (CC) loops [9]. The DVC loop of the VSC is responsible for generating *d*-axis current reference for the CC loop. The stability of current control in VSCs with filters has been extensively investigated [10], [11], highlighting the significant influence of time delays in the digital control system. Furthermore, recent studies have explored the dynamic effects of the grid synchronization loop [12], [13]. These investigations have revealed that the phase-locked loop (PLL) plays a crucial role in determining the stability of weak-grid-tied VSCs.

When considering the dynamics of the DC-link voltage in the stability analysis of grid connected VSC, reference [14] conducts a comparative analysis of the stability influence of different controllers under weak grid conditions. However, it primarily focuses on the analysis of the CC loop without analyzing the effects introduced by the DVC. The impact of control loop parameters on the stability of VSC is investigated using the input admittance matrix. Specifically, the effects of

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selecting large bandwidth values for DVC and PLL control are examined in [15]. In [16], the influence of PLL dynamics on the stability of DVC in weak-grid-tied VSC is investigates, and it reveals that PLL has a phase lag effect on DVC. In [17], an analysis is presented on the impact characteristics of DVC parameters on grid-tied VSCs. The study constructs a loop gain model, which reveals that DVC can potentially induce low-frequency oscillations in the rectifier mode and high-frequency oscillations in the inverter mode.

In [18] and [19], a mathematical model of weak-grid-tied VSCs is developed, considering a single-input single-output configuration, to analyze the stability impact of the DVC parameters. However, the influence of the CC parameters on system stability is not examined. Based on that, a subsequent study in [20] investigates the effects of both DVC and CC parameter variations on the stability of VSCs. Nonetheless, the different impacts of the DVC and CC parameters are not explicitly identified in the analysis.

It is worth noting that the existing impedance modeling and stability analysis methods, which consider DVC, primarily focus on source or load converters where the AC- and DC-side dynamics are modeled separately. However, there is limited knowledge regarding interlinking converters that serve as interface media for connecting AC and DC grids. In contrast to source/load converters, the modeling of interlinking converters should consider the coupling interaction between the AC- and DC-sides [21]. Therefore, it is essential to further explore and understand the unique challenges posed by interlinking converters in terms of impedance modeling and stability analysis, taking into account the interaction between the AC- and DC-sides.

Furthermore, while it is possible to incorporate AC- and DC-side dynamics into these models, the AC-side admittance-based model represents typically a two-port model that relates AC-side voltages and currents. On the other hand, the DC-side admittance-based model is typically a single-port model that relates DC-side voltage and current [22], [23]. These models offer separate representations of the AC- and DC-sides, focusing on their respective voltage and current relationships. Therefore, a three-port transfer admittance-based matrix model of VSC relating AC- and DC-side voltages and currents is necessary to study the weak-grid-tied interlinking VSC from the nodal admittance matrix approach. Three-port transfer admittance-based matrix models that consider AC and DC dynamics have recently been presented to apply in hybrid AC/DC grid [21], [24]. However, they neither consider the detailed three-port admittance-based model with DVC nor are applied to identify the different impacts of the DVC and CC parameters.

The three-port transfer admittance-based matrix model can be employed to analyze the system stability by nodal admittance matrix including the relationships between AC- and DC-side voltages and currents. Recent studies have introduced three-port transfer admittance-based matrix models that consider the dynamics of both the AC- and DC-sides, making them suitable for hybrid AC/DC grid studies [20], [25]. However, these existing models either lack the inclusion of a detailed three-port admittance-based model with DVC or fail to explore the different impacts of the DVC and CC parameters. Thus, there is still a need for further research to develop a comprehensive three-port VSC model that includes DVC and assesses the different impacts of the DVC and CC parameters.

To address the different impacts on the stability of the DVC and CC parameters, a VSC three-port admittance-based model is established to reveal the mechanism on forming positive and negative feedback effects. The main advantages of this paper are listed as follows.

1) A VSC three-port admittance-based model under DVC mode is presented. The model systematically and rigorously extends the three-port transfer admittance-based matrix models in [21], [24] and [25] by considering the AC- and DC-side interactions.

2) The VSC three-port equivalent small-signal block diagram model is further simplified, which can be applied for revealing the mechanism that the CC loop through the hybrid AC/DC impedance and PLL forms positive and negative feedback effects in the DVC loop.

3) The different stability characteristics of the voltage control loop and current control loop parameters for VSC are analyzed based on the three-port admittance-based model. Compared to adjusting the voltage control loop parameters with the dynamic regulation characteristics, it reveals that it is more sensitive for system stability by changing the parameters of the current inner loop controller, and the stability may be decreased by positive and negative feedback effects counteraction.

The rest of the paper is organized as follows. In Section II, an equivalent transformation is obtained for the three-port converter control block diagram model with current positive and negative feedback effects used to indicate the stability. Section III analyzes the differences impacts on the VSC stability with parameters of the DVC and CC loops. In Section IV, experimental results are presented to validate the theoretical analysis, whereas Section V concludes the paper.

II. THREE-PORT GRID-TIED INTERLINKING VSC SYSTEM MODELING UNDER DC VOLTAGE CONTROL MODE

Figure 1 depicts the schematic of a typical scenario, illustrating the connection of an interlinking VSC to a weak power grid and DC grid. In the power stage, the interlinking VSC is equipped with an LCL filter (L_1, C_f and L_2) and an AC-side damping resistor (R_c).

Additionally, a DC-link capacitor (C_{dc}) is present on the DC-side. The VSC control system consists of the CC and DVC loops. The phase angle is tracked using a synchronous reference frame phase-locked loop (SRF-PLL). The DVC loop generates the current reference for active power while a zero value is assumed for the reactive power current reference.

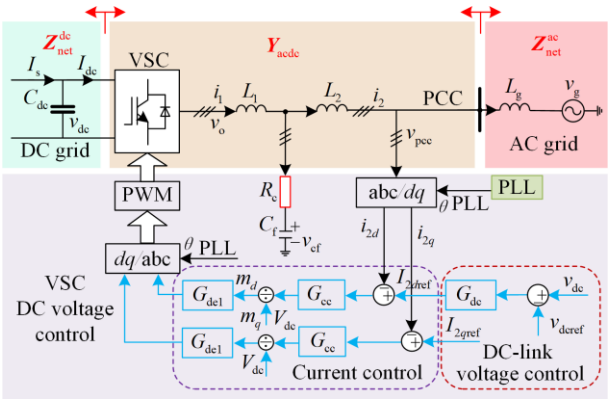


Fig. 1. Topology and control block of a three-phase weak-grid-tied interlinking VSC system.

A. AC Grid Modeling

According to Fig. 1, the small-signal voltage balance across the converter's LCL filter can be expressed in the *d*-*q* frame using Laplace transformation [20], as:

$$\begin{bmatrix}\Delta v_{od}^{\mathrm{s}}\\ \Delta v_{oq}^{\mathrm{s}}\end{bmatrix}=\boldsymbol{Z}_1\begin{bmatrix}\Delta i_{1d}^{\mathrm{s}}\\ \Delta i_{1q}^{\mathrm{s}}\end{bmatrix}+\begin{bmatrix}\Delta v_{\mathrm{cf}d}^{\mathrm{s}}\\ \Delta v_{\mathrm{cf}q}^{\mathrm{s}}\end{bmatrix}+\boldsymbol{Z}_{\mathrm{Rc}}\left(\begin{bmatrix}\Delta i_{1d}^{\mathrm{s}}\\ \Delta i_{1q}^{\mathrm{s}}\end{bmatrix}-\begin{bmatrix}\Delta i_{2d}^{\mathrm{s}}\\ \Delta i_{2q}^{\mathrm{s}}\end{bmatrix}\right) \tag{1}$$

$$\begin{bmatrix}\Delta i_{1d}^{\mathrm{s}}\\ \Delta i_{1q}^{\mathrm{s}}\end{bmatrix}-\begin{bmatrix}\Delta i_{2d}^{\mathrm{s}}\\ \Delta i_{2q}^{\mathrm{s}}\end{bmatrix}=\underbrace{\begin{bmatrix}sC_f & -\omega C_f\\ \omega C_f & sC_f\end{bmatrix}}_{\boldsymbol{Y}_{\mathrm{C}}}\begin{bmatrix}\Delta v_{\mathrm{cf}d}^{\mathrm{s}}\\ \Delta v_{\mathrm{cf}q}^{\mathrm{s}}\end{bmatrix} \tag{2}$$

$$\begin{bmatrix}\Delta v_{\mathrm{pcc}d}^{\mathrm{s}}\\ \Delta v_{\mathrm{pcc}q}^{\mathrm{s}}\end{bmatrix}=\begin{bmatrix}\Delta v_{\mathrm{cf}d}^{\mathrm{s}}\\ \Delta v_{\mathrm{cf}q}^{\mathrm{s}}\end{bmatrix}+\boldsymbol{Z}_{\mathrm{Rc}}\left(\begin{bmatrix}\Delta i_{1d}^{\mathrm{s}}\\ \Delta i_{1q}^{\mathrm{s}}\end{bmatrix}-\begin{bmatrix}\Delta i_{2d}^{\mathrm{s}}\\ \Delta i_{2q}^{\mathrm{s}}\end{bmatrix}\right)-\boldsymbol{Z}_2\begin{bmatrix}\Delta i_{2d}^{\mathrm{s}}\\ \Delta i_{2q}^{\mathrm{s}}\end{bmatrix} \tag{3}$$

$$\begin{cases}\boldsymbol{Z}_1=\begin{bmatrix}L_1 s & -\omega L_1\\ \omega L_1 & L_1 s\end{bmatrix}\\ \boldsymbol{Z}_2=\begin{bmatrix}L_2 s & -\omega L_2\\ \omega L_2 & L_2 s\end{bmatrix}\\ \boldsymbol{Z}_{\mathrm{RC}}=\begin{bmatrix}R_{\mathrm{c}} & 0\\ 0 & R_{\mathrm{c}}\end{bmatrix}\end{cases} \tag{4}$$

where $\Delta v_{od}^{\mathrm{s}}$ and $\Delta v_{oq}^{\mathrm{s}}$ are small-signal values of *d*-axis and *q*-axis VSC output voltages v_{od} and v_{oq} in the grid frame, respectively; $\Delta i_{1d}^{\mathrm{s}}$ and $\Delta i_{1q}^{\mathrm{s}}$ are small-signal values of *d*-axis and *q*-axis VSC output currents i_{1d} and i_{1q} in the grid frame, respectively; $\Delta v_{\mathrm{cf}d}^{\mathrm{s}}$ and $\Delta v_{\mathrm{cf}q}^{\mathrm{s}}$ are small-signal values of *d*-axis and *q*-axis filter capacitor voltages $v_{\mathrm{cf}d}$ and $v_{\mathrm{cf}q}$ respectively; $\Delta i_{2d}^{\mathrm{s}}$ and $\Delta i_{2q}^{\mathrm{s}}$ are small-signal values of *d*-axis and *q*-axis grid-tied currents i_{2d} and i_{2q} in the grid frame, respectively.

By substituting (2) into (1), (3) and (4), the followings can be derived:

$$\boldsymbol{Y}_{\mathrm{out1}}\begin{bmatrix}\Delta v_{\mathrm{pcc}d}^{\mathrm{s}}\\ \Delta v_{\mathrm{pcc}q}^{\mathrm{s}}\end{bmatrix}+\boldsymbol{G}_{\mathrm{id1}}\begin{bmatrix}\Delta v_{od}^{\mathrm{s}}\\ \Delta v_{oq}^{\mathrm{s}}\end{bmatrix}=\begin{bmatrix}\Delta i_{2d}^{\mathrm{s}}\\ \Delta i_{2q}^{\mathrm{s}}\end{bmatrix} \tag{5}$$

where $\Delta v_{\mathrm{pcc}d}^{\mathrm{s}}$ and $\Delta v_{\mathrm{pcc}q}^{\mathrm{s}}$ are small-signal values of *d*-axis and *q*-axis voltages at the point of common coupling $v_{\mathrm{pcc}d}$ and $v_{\mathrm{pcc}q}$ in the grid frame, respectively; and there are:

$$\begin{cases}\boldsymbol{Y}_{\mathrm{out1}}=-\boldsymbol{G}_{\mathrm{id1}}\left[\boldsymbol{Z}_1\boldsymbol{Y}_{\mathrm{RC}}\left(\boldsymbol{Z}_1\boldsymbol{Y}_{\mathrm{C}}+\boldsymbol{I}_{2\times2}\right)^{-1}+\boldsymbol{I}_{2\times2}\right]\\ \boldsymbol{G}_{\mathrm{id1}}=\left[\boldsymbol{Z}_1\boldsymbol{Y}_{\mathrm{RC}}\left(\boldsymbol{Z}_1\boldsymbol{Y}_{\mathrm{RC}}+\boldsymbol{I}_{2\times2}\right)^{-1}\boldsymbol{Z}_2+\boldsymbol{Z}_2+\boldsymbol{Z}_1\right]^{-1}\end{cases} \tag{6}$$

where $\boldsymbol{I}_{2\times2}$ represents a 2nd-order identity matrix.

The hybrid AC/DC small-signal admittance model of the VSC is derived by incorporating the DC-side variables such as DC voltage and current, as:

$$\boldsymbol{Y}_{\mathrm{out}}\begin{bmatrix}\Delta v_{\mathrm{pcc}d}^{\mathrm{s}}\\ \Delta v_{\mathrm{pcc}q}^{\mathrm{s}}\\ \Delta i_{\mathrm{dc}}\end{bmatrix}+\boldsymbol{G}_{\mathrm{id}}\begin{bmatrix}\Delta v_{od}^{\mathrm{s}}\\ \Delta v_{oq}^{\mathrm{s}}\\ \Delta v_{\mathrm{dc}}\end{bmatrix}=\begin{bmatrix}\Delta i_{2d}^{\mathrm{s}}\\ \Delta i_{2q}^{\mathrm{s}}\\ \Delta v_{\mathrm{dc}}\end{bmatrix} \tag{7}$$

where Δv_{dc} is small-signal value of DC-link voltage of the VSC (v_{dc}); Δi_{dc} is small-signal value of input current of the VSC (i_{dc}); $\boldsymbol{Y}_{\mathrm{out}}$ and $\boldsymbol{G}_{\mathrm{id}}$ are shown as follows:

$$\begin{cases}\boldsymbol{Y}_{\mathrm{out}}=\begin{bmatrix}\boldsymbol{Y}_{\mathrm{out1}} & \boldsymbol{0}_{2\times1}\\ \boldsymbol{0}_{1\times2} & 0\end{bmatrix}\\ \boldsymbol{G}_{\mathrm{id}}=\begin{bmatrix}\boldsymbol{G}_{\mathrm{id1}} & \boldsymbol{0}_{2\times1}\\ \boldsymbol{0}_{1\times2} & 1\end{bmatrix}\end{cases} \tag{8}$$

B. AC/DC Converter Modeling

The modulation function m_{dq} is employed to establish the relationship between v_{odq} and v_{dc} [12], so the corresponding small signal variables are interconnected as:

$$\begin{bmatrix}v_{od}^{\mathrm{s}}\\ v_{oq}^{\mathrm{s}}\end{bmatrix}=u_{\mathrm{dc}}\begin{bmatrix}m_d^{\mathrm{s}}\\ m_q^{\mathrm{s}}\end{bmatrix} \tag{9}$$

$$\begin{bmatrix}\Delta v_{od}^{\mathrm{s}}\\ \Delta v_{oq}^{\mathrm{s}}\end{bmatrix}=V_{\mathrm{dc}}\begin{bmatrix}\Delta m_d^{\mathrm{s}}\\ \Delta m_q^{\mathrm{s}}\end{bmatrix}+\Delta v_{\mathrm{dc}}\begin{bmatrix}M_d^{\mathrm{s}}\\ M_q^{\mathrm{s}}\end{bmatrix} \tag{10}$$

where V_{dc} is steady-state value of v_{dc} ; Δm_d^{s} and Δm_q^{s} are small-signal values of m_d and m_q in the grid frame; M_d^{s} and M_q^{s} are steady-state values of m_d and m_q in the grid frame.

In order to account for the dynamic influence of the DC bus voltage, an ideal lossless model of the VSC is assumed to simplify the modeling process. Consequently, the power balance constraint between the DC- and AC-sides of the VSC can be expressed as:

$$P = i_{\mathrm{dc}} v_{\mathrm{dc}} = (i_{1d}^{\mathrm{s}} m_d^{\mathrm{s}} + i_{1q}^{\mathrm{s}} m_q^{\mathrm{s}}) v_{\mathrm{dc}} \tag{11}$$

where

$$i_{\mathrm{dc}} = i_{1d}^{\mathrm{s}} m_d^{\mathrm{s}} + i_{1q}^{\mathrm{s}} m_q^{\mathrm{s}} \tag{12}$$

The dynamic equation for the DC-link voltage and the input DC current to the VSC can be formulated as:

$$sC_{\mathrm{dc}} v_{\mathrm{dc}} = I_{\mathrm{o}} - i_{\mathrm{dc}} \tag{13}$$

$$I_{\mathrm{o}} = \frac{P}{v_{\mathrm{dc}}} \tag{14}$$

Combining (13) and (14), Δi_{dc} is given as:

$$\Delta i_{\mathrm{dc}} = \underbrace{-\left(sC_{\mathrm{dc}} + \frac{P}{V_{\mathrm{dc}}^2}\right)}_{Y_{\mathrm{dc}}} \Delta v_{\mathrm{dc}} \tag{15}$$

Linearizing (12) and using (15), there is:

$$\begin{bmatrix} \Delta v_{\mathrm{dc}} \\ 0 \end{bmatrix} = \boldsymbol{H}_1(s) \begin{bmatrix} \Delta i_{1d}^{\mathrm{s}} \\ \Delta i_{1q}^{\mathrm{s}} \end{bmatrix} - \boldsymbol{H}_2(s) \begin{bmatrix} \Delta m_d^{\mathrm{s}} \\ \Delta m_q^{\mathrm{s}} \end{bmatrix} \tag{16}$$

where

$$\begin{cases} \boldsymbol{H}_1 = -\dfrac{1}{Y_{\mathrm{dc}}} \begin{bmatrix} M_d & M_q \\ 0 & 0 \end{bmatrix} \\ \boldsymbol{H}_2 = \dfrac{1}{Y_{\mathrm{dc}}} \begin{bmatrix} I_{1d} & I_{1q} \\ 0 & 0 \end{bmatrix} \end{cases} \tag{17}$$

From (1)–(4), (10), (16) and (17), equation (18) is obtained as:

$$\begin{bmatrix} \Delta v_{od}^{\mathrm{s}} \\ \Delta v_{oq}^{\mathrm{s}} \\ \Delta v_{\mathrm{dc}} \end{bmatrix} = \boldsymbol{G}_{\mathrm{du}} \begin{bmatrix} \Delta m_d^{\mathrm{s}} \\ \Delta m_q^{\mathrm{s}} \\ \Delta i_{\mathrm{dc}} \end{bmatrix} + \boldsymbol{G}_{\mathrm{iu}} \begin{bmatrix} \Delta i_{2d}^{\mathrm{s}} \\ \Delta i_{2q}^{\mathrm{s}} \\ \Delta v_{\mathrm{dc}} \end{bmatrix} + \boldsymbol{G}_{\mathrm{vu}} \begin{bmatrix} \Delta v_{\mathrm{pcc}d}^{\mathrm{s}} \\ \Delta v_{\mathrm{pcc}q}^{\mathrm{s}} \\ \Delta i_{\mathrm{dc}} \end{bmatrix} \tag{18}$$

where

$$\begin{cases} \boldsymbol{G}_{\mathrm{du}} = \begin{bmatrix} V_{\mathrm{dc}} & 0 & 0 \\ 0 & V_{\mathrm{dc}} & 0 \\ -\dfrac{1}{\boldsymbol{Y}_{\mathrm{dc}}} I_{1d}^{\mathrm{s}} & \dfrac{1}{\boldsymbol{Y}_{\mathrm{dc}}} I_{1q}^{\mathrm{s}} & 0 \end{bmatrix} \\ \boldsymbol{G}_{\mathrm{iu}} = \begin{bmatrix} \boldsymbol{0}_{1\times 2} & 0 \\ \boldsymbol{G}_{\mathrm{iu1}} & \boldsymbol{0}_{2\times 1} \end{bmatrix} \\ \boldsymbol{G}_{\mathrm{vu}} = \begin{bmatrix} \boldsymbol{0}_{1\times 2} & 0 \\ \boldsymbol{G}_{\mathrm{vu1}} & \boldsymbol{0}_{2\times 1} \end{bmatrix} \\ \boldsymbol{G}_{\mathrm{iu1}} = \boldsymbol{H}_1 \boldsymbol{Y}_{\mathrm{C}} (\boldsymbol{Z}_{\mathrm{L}_1} \boldsymbol{Y}_{\mathrm{C}} + \boldsymbol{I}_{2\times 2})^{-1} \boldsymbol{Z}_{\mathrm{L}_2} + \boldsymbol{H}_1 \\ \boldsymbol{G}_{\mathrm{vu1}} = \boldsymbol{H}_1 \boldsymbol{Y}_{\mathrm{C}} (\boldsymbol{Z}_{\mathrm{L}_1} \boldsymbol{Y}_{\mathrm{C}} + \boldsymbol{I}_{2\times 2})^{-1} \end{cases} \tag{19}$$

C. SRF-PLL Modeling

When the system operates in a steady state, its *d-q* frame aligns with the controller's *d-q* frame. However, when a small signal perturbation is introduced to the system, there exists a phase difference between these two frames due to SRF-PLL. By considering the phase difference between the controller and system frames, along with the PLL structure, the output angle during the perturbation period $\Delta\theta$ can be expressed as:

$$\Delta\theta = \frac{G_{\mathrm{PLL}}}{s + V_{\mathrm{pcc}d}^{\mathrm{s}} G_{\mathrm{PLL}}} \Delta v_{\mathrm{pcc}q}^{\mathrm{s}} = G_{\mathrm{pll}} \Delta v_{\mathrm{pcc}q}^{\mathrm{s}} \tag{20}$$

where the transfer function of the SRF-PLL is denoted as $G_{\mathrm{PLL}} = k_{p\mathrm{pll}} + k_{i\mathrm{pll}}/s$.

Hence, based on (20), the transformation of the PCC current vector and modulation function from the controller's *d-q* frame to the system's *d-q* frame can be summarized as:

$$\begin{bmatrix} \Delta i_{2d}^{\mathrm{c}} \\ \Delta i_{2q}^{\mathrm{c}} \end{bmatrix} = \begin{bmatrix} \Delta i_{2d}^{\mathrm{s}} \\ \Delta i_{2q}^{\mathrm{s}} \end{bmatrix} + \begin{bmatrix} 0 & G_{\mathrm{pll}} I_{2q}^{\mathrm{s}} \\ 0 & -G_{\mathrm{pll}} I_{2d}^{\mathrm{s}} \end{bmatrix} \begin{bmatrix} \Delta v_{\mathrm{pcc}d}^{\mathrm{s}} \\ \Delta v_{\mathrm{pcc}q}^{\mathrm{s}} \end{bmatrix} \tag{21}$$

$$\begin{bmatrix} \Delta m_d^{\mathrm{s}} \\ \Delta m_q^{\mathrm{s}} \end{bmatrix} = \begin{bmatrix} \Delta m_d^{\mathrm{c}} \\ \Delta m_q^{\mathrm{c}} \end{bmatrix} + \begin{bmatrix} 0 & -G_{\mathrm{pll}} M_q^{\mathrm{s}} \\ 0 & G_{\mathrm{pll}} M_d^{\mathrm{s}} \end{bmatrix} \begin{bmatrix} \Delta v_{\mathrm{pcc}d}^{\mathrm{s}} \\ \Delta v_{\mathrm{pcc}q}^{\mathrm{s}} \end{bmatrix} \tag{22}$$

where $\Delta i_{2d}^{\mathrm{c}}$ and $\Delta i_{2q}^{\mathrm{c}}$ are small-signal values of i_{2d} and i_{2q} in the controller frame; Δm_d^{c} and Δm_q^{c} are small-signal values of m_d and m_q in the controller frame.

The small-signal representations of the current and modulation function are described by incorporating the DC voltage and current, as:

$$\begin{bmatrix} \Delta i_{2d}^{\mathrm{c}} \\ \Delta i_{2q}^{\mathrm{c}} \\ \Delta v_{\mathrm{dc}} \end{bmatrix} = \begin{bmatrix} \Delta i_{2d}^{\mathrm{s}} \\ \Delta i_{2q}^{\mathrm{s}} \\ \Delta v_{\mathrm{dc}} \end{bmatrix} + \boldsymbol{G}_{\mathrm{PLL}}^{\mathrm{i}} \begin{bmatrix} \Delta v_{\mathrm{pcc}d}^{\mathrm{s}} \\ \Delta v_{\mathrm{pcc}q}^{\mathrm{s}} \\ \Delta i_{\mathrm{dc}} \end{bmatrix} \tag{23}$$

$$\begin{bmatrix} \Delta m_d^{\mathrm{s}} \\ \Delta m_q^{\mathrm{s}} \\ \Delta v_{\mathrm{dc}} \end{bmatrix} = \begin{bmatrix} \Delta m_d^{\mathrm{c}} \\ \Delta m_q^{\mathrm{c}} \\ 0 \end{bmatrix} + \boldsymbol{G}_{\mathrm{PLL}}^{\mathrm{d}} \begin{bmatrix} \Delta v_{\mathrm{pcc}d}^{\mathrm{s}} \\ \Delta v_{\mathrm{pcc}q}^{\mathrm{s}} \\ \Delta i_{\mathrm{dc}} \end{bmatrix} \tag{24}$$

where

$$\begin{cases} \boldsymbol{G}_{\mathrm{PLL}}^{\mathrm{i}} = \begin{bmatrix} 0 & G_{\mathrm{pll}} I_{2q}^{\mathrm{s}} & 0 \\ 0 & -G_{\mathrm{pll}} I_{2d}^{\mathrm{s}} & 0 \\ 0 & 0 & 0 \end{bmatrix} \\ \boldsymbol{G}_{\mathrm{PLL}}^{\mathrm{d}} = \begin{bmatrix} 0 & -G_{\mathrm{pll}} M_q^{\mathrm{s}} & 0 \\ 0 & G_{\mathrm{pll}} M_d^{\mathrm{s}} & 0 \\ 0 & 0 & -1/Y_{\mathrm{dc}} \end{bmatrix} \end{cases} \tag{25}$$

D. Control Loop Modeling

The control laws of the CC and DVC loops in the controller's *d-q* frame are considered as:

$$\begin{bmatrix}\Delta i^{\mathrm{c}}_{2d\mathrm{ref}}\\ \Delta i^{\mathrm{c}}_{2q\mathrm{ref}}\end{bmatrix}=\begin{bmatrix}G_{\mathrm{dc}}\\ 0\end{bmatrix}\begin{bmatrix}\Delta v_{\mathrm{dc}}\\ 0\end{bmatrix} \tag{26}$$

$$\begin{bmatrix}\Delta m^{\mathrm{c}}_{d}\\ \Delta m^{\mathrm{c}}_{q}\end{bmatrix}=G_{\mathrm{nor}}\begin{bmatrix}G_{\mathrm{cc}} & 0\\ 0 & G_{\mathrm{cc}}\end{bmatrix}\left(\begin{bmatrix}\Delta i^{\mathrm{c}}_{2d\mathrm{ref}}\\ \Delta i^{\mathrm{c}}_{2q\mathrm{ref}}\end{bmatrix}-\begin{bmatrix}\Delta i^{\mathrm{c}}_{2d}\\ \Delta i^{\mathrm{c}}_{2q}\end{bmatrix}\right) \tag{27}$$

where $G_{\mathrm{dc}}=k_{\mathrm{pdc}}+k_{\mathrm{idc}}/s$ denotes the PI controller of the DVC; $G_{\mathrm{cc}}=k_{\mathrm{pcc}}+k_{\mathrm{icc}}/s$ is the PI controller of the CC; and $\boldsymbol{G}_{\mathrm{nor}}=1/V_{\mathrm{dc}}$ is the normalization matrix.

Embedding the DC voltage and current, the current and modulation function can be described as:

$$\begin{bmatrix}\Delta i^{\mathrm{c}}_{2d\mathrm{ref}}\\ \Delta i^{\mathrm{c}}_{2q\mathrm{ref}}\\ \Delta v_{\mathrm{dc}}\end{bmatrix}=\begin{bmatrix}0 & 0 & G_{\mathrm{dc}}\\ 0 & 0 & 0\\ 0 & 0 & 0\end{bmatrix}\begin{bmatrix}0\\ 0\\ \Delta v_{\mathrm{dc}}\end{bmatrix} \tag{28}$$

$$\begin{bmatrix}\Delta m^{\mathrm{c}}_{d}\\ \Delta m^{\mathrm{c}}_{q}\\ 0\end{bmatrix}=\boldsymbol{G}_{\mathrm{nor}}\begin{bmatrix}G_{\mathrm{cc}} & 0 & 0\\ 0 & G_{\mathrm{cc}} & 0\\ 0 & 0 & 0\end{bmatrix}\left(\begin{bmatrix}\Delta i^{\mathrm{c}}_{2d\mathrm{ref}}\\ \Delta i^{\mathrm{c}}_{2q\mathrm{ref}}\\ \Delta v_{\mathrm{dc}}\end{bmatrix}-\begin{bmatrix}\Delta i^{\mathrm{c}}_{2d}\\ \Delta i^{\mathrm{c}}_{2q}\\ \Delta v_{\mathrm{dc}}\end{bmatrix}\right) \tag{29}$$

The small-signal block diagram of the VSC operating under DVC mode, based on (16)–(29), is illustrated in Fig. 2, with

$$\boldsymbol{G}_{\mathrm{1}}=\begin{bmatrix}0 & 0 & 0\\ 0 & 0 & 0\\ 0 & 0 & 1\end{bmatrix} \tag{30}$$

$$\boldsymbol{G}_{\mathrm{del}}=\begin{bmatrix}\dfrac{1-0.5T_{\mathrm{del}}s}{1+0.5T_{\mathrm{del}}s} & 0 & 0\\ 0 & \dfrac{1-0.5T_{\mathrm{del}}s}{1+0.5T_{\mathrm{del}}s} & 0\\ 0 & 0 & 0\end{bmatrix} \tag{31}$$

$$\boldsymbol{G}_{\mathrm{nor}}=\begin{bmatrix}\dfrac{1}{V_{\mathrm{dc}}} & 0 & 0\\ 0 & \dfrac{1}{V_{\mathrm{dc}}} & 0\\ 0 & 0 & 0\end{bmatrix} \tag{32}$$

where $\boldsymbol{G}_{\mathrm{del}}$ represents the time delay (T_{del}) by digital control and PWM [12].

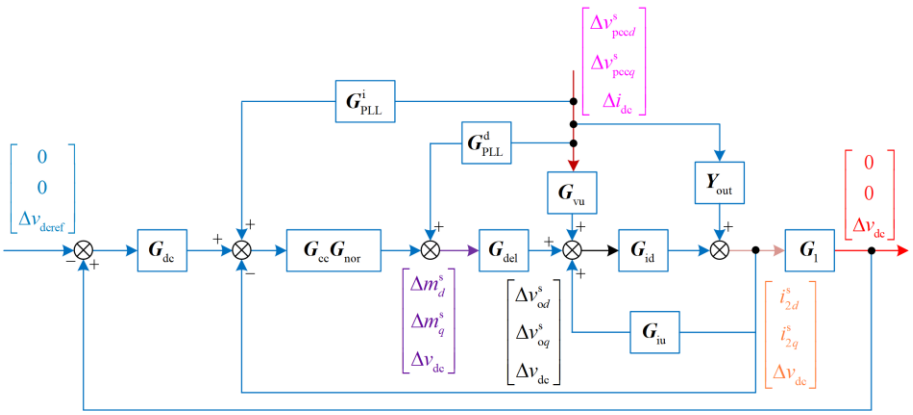


Fig.2. Three-port small-signal model of the converter under the DC-link voltage control mode.

Using series equivalent transformation on the control block diagram for Fig. 2, an equivalent transformation can be obtained for the three-port converter control block diagram model with current positive and negative feedback effects, as shown in Fig. 3. The $\boldsymbol{G}_{\mathrm{F}}$ is calculated by:

$$\begin{cases}\boldsymbol{G}_{\mathrm{C}}=\boldsymbol{G}_{\mathrm{vu}}+\dfrac{\boldsymbol{Y}_{\mathrm{out}}}{\boldsymbol{G}_{\mathrm{id}}}\\ \boldsymbol{G}_{\mathrm{D}}=\dfrac{\boldsymbol{G}_{\mathrm{id}}}{\boldsymbol{I}_{3\times3}-\boldsymbol{G}_{\mathrm{id}}\boldsymbol{G}_{\mathrm{iu}}}\\ \boldsymbol{G}_{\mathrm{E}}=\dfrac{\boldsymbol{Z}_{\mathrm{net}}}{\boldsymbol{Z}_{\mathrm{net}}+\boldsymbol{G}_{\mathrm{D}}\boldsymbol{G}_{\mathrm{C}}}\\ \boldsymbol{G}_{\mathrm{F}}=\boldsymbol{G}_{\mathrm{E}}\boldsymbol{G}_{\mathrm{D}}\end{cases} \tag{33}$$

where $\boldsymbol{Z}_{\mathrm{net}}$ is the hybrid admittance of the AC and DC grids.

From Fig. 3, it can be noticed that the CC PI controller generates a positive feedback loop and a negative feedback loop in the DVC loop. Nevertheless, the DVC loop is solely present in the forward path of the VSC small-signal control block diagram. The control structure highlights the 'dual role' played by the CC loop in the stability of the DVC loop. The positive feedback loop introduced by the CC loop can diminish the stability of the VSC system, whereas the negative feedback loop contributes to the stability of the system. In simpler terms, when tuning the parameters of the CC loop, there is a phenomenon of mutual cancellation between its positive and negative

feedback effects. If the negative feedback effect surpasses the positive feedback effect, the stability of the weak-grid-tied system is enhanced. Otherwise, the system's stability is weakened.

Noting that the positive feedback effect in the system is mainly induced by the SRF-PLL and $\boldsymbol{Z}_{\text{net}}$. In Fig. 3, if $\boldsymbol{Z}_{\text{net}} = \boldsymbol{0}_{3\times3}$, both $\boldsymbol{G}_{\text{PLL}}^{\text{d}}$ and $\boldsymbol{G}_{\text{PLL}}^{\text{i}}$ will not be excited, and the positive feedback loop $\boldsymbol{G}_{\text{nor}}\boldsymbol{G}_{\text{cc}}\boldsymbol{G}_{\text{PLL}}^{\text{d}}\boldsymbol{Z}_{\text{net}} + \boldsymbol{G}_{\text{PLL}}^{\text{i}}\boldsymbol{Z}_{\text{net}}$ will not be formed. Therefore, when considering the influence of $\boldsymbol{Z}_{\text{net}}$, the positive and negative feedback effects will be formed in the VSC system.

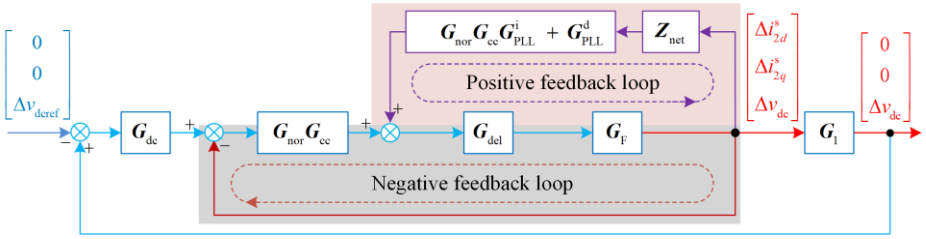


Fig. 3. Three-port small-signal model of the converter with current positive and negative feedback loop effect.

III. Stability Impact Analysis of the Positive and Negative Feedback Loop Effects

Due to the formation of positive and negative feedback effects in the DVC loop, this control structure will lead to different impacts on the VSC stability with parameters of the DVC and CC loops. To facilitate the analysis of discrepancies, an admittance model of the system is needed to analyze the parameters' influence of the DVC and CC loops on the system stability.

The relationship between the input voltage and output current of the converter can be expressed by:

$$\begin{bmatrix}\Delta i_{2d}^{\text{s}}\\ \Delta i_{2q}^{\text{s}}\\ \Delta v_{\text{dc}}\end{bmatrix} = \boldsymbol{Y}_{\text{acdc}}\begin{bmatrix}\Delta v_{\text{pcc}d}^{\text{s}}\\ \Delta v_{\text{pcc}q}^{\text{s}}\\ \Delta i_{\text{dc}}\end{bmatrix} \tag{34}$$

where $\boldsymbol{Y}_{\text{acdc}}$ represents the hybrid AC/DC admittance of the VSC operating in DVC mode, expressed as:

$$\begin{aligned}\boldsymbol{Y}_{\text{acdc}} = &-\left[\boldsymbol{I}_{3\times3} - \boldsymbol{G}_{\text{iu}}\boldsymbol{G}_{\text{id}} + \boldsymbol{G}_{\text{id}}\boldsymbol{G}_{\text{del}}\boldsymbol{G}_{\text{du}}\boldsymbol{G}_{\text{nor}}\boldsymbol{G}_{\text{cc}}\right]^{-1}\times\\ &\begin{bmatrix}\boldsymbol{Y}_{\text{out}} + \boldsymbol{G}_{\text{id}}\boldsymbol{G}_{\text{del}}\boldsymbol{G}_{\text{du}}\boldsymbol{G}_{\text{PLL}}^{\text{d}} +\\ \boldsymbol{G}_{\text{id}}\boldsymbol{G}_{\text{vu}} - \boldsymbol{G}_{\text{id}}\boldsymbol{G}_{\text{del}}\boldsymbol{G}_{\text{du}}\boldsymbol{G}_{\text{nor}}\boldsymbol{G}_{\text{cc}}\boldsymbol{G}_{\text{PLL}}^{\text{i}} -\\ \boldsymbol{G}_{\text{id}}\boldsymbol{G}_{\text{del}}\boldsymbol{G}_{\text{du}}\boldsymbol{G}_{\text{nor}}\boldsymbol{G}_{\text{cc}}\boldsymbol{G}_{\text{vc}}\end{bmatrix}\end{aligned} \tag{35}$$

A. Stability Analysis Based on Three Port Impedance Model

In this paper, the system is divided into three parts based on the point of common coupling (PCC) on the AC- and DC-sides, i.e., the DC-link voltage controlled converter, the AC grid, and the DC grid, as depicted in Fig. 1. The small-signal representation of the AC grid can be expressed as:

$$\begin{bmatrix}\Delta v_{\text{pcc}d}^{\text{s}}\\ \Delta v_{\text{pcc}q}^{\text{s}}\end{bmatrix} = \begin{bmatrix}\Delta v_{gd}^{\text{s}}\\ \Delta v_{gq}^{\text{s}}\end{bmatrix} + \begin{bmatrix}sL_{\text{g}} & -\omega L_{\text{g}}\\ \omega L_{\text{g}} & sL_{\text{g}}\end{bmatrix}\begin{bmatrix}\Delta i_{2d}^{\text{s}}\\ \Delta i_{2q}^{\text{s}}\end{bmatrix} \tag{36}$$

Based on (15) and (36), the variables of the AC- and DC-sides can be combined and modeled together as:

$$\begin{bmatrix}\Delta v_{\text{pcc}d}^{\text{s}}\\ \Delta v_{\text{pcc}q}^{\text{s}}\\ \Delta i_{\text{dc}}\end{bmatrix} = \begin{bmatrix}\Delta v_{gd}^{\text{s}}\\ \Delta v_{gq}^{\text{s}}\\ 0\end{bmatrix} + \boldsymbol{Z}_{\text{net}}\begin{bmatrix}\Delta i_{2d}^{\text{s}}\\ \Delta i_{2q}^{\text{s}}\\ \Delta v_{\text{dc}}\end{bmatrix} \tag{37}$$

where

$$\boldsymbol{Z}_{\text{net}} = \left[\begin{array}{c|c}\boldsymbol{Z}_{\text{net}}^{\text{ac}} & \boldsymbol{0}\\ \hline \boldsymbol{0} & \boldsymbol{Z}_{\text{net}}^{\text{dc}}\end{array}\right] = \begin{bmatrix}sL_{\text{g}} & -\omega L_{\text{g}} & 0\\ \omega L_{\text{g}} & sL_{\text{g}} & 0\\ 0 & 0 & Y_{\text{dc}}\end{bmatrix} \tag{38}$$

Combining (35) and (38), the small-signal model of the system is expressed by:

$$\begin{bmatrix}\Delta v_{\text{pcc}d}^{\text{s}}\\ \Delta v_{\text{pcc}q}^{\text{s}}\\ \Delta i_{\text{dc}}\end{bmatrix} = \left(\boldsymbol{I}_{3\times3} + \boldsymbol{Y}_{\text{acdc}}\boldsymbol{Z}_{\text{net}}\right)^{-1}\begin{bmatrix}\Delta v_{gd}^{\text{s}}\\ \Delta v_{gq}^{\text{s}}\\ 0\end{bmatrix} \tag{39}$$

The minor loop gain of the system is defined as:

$$\boldsymbol{L} = \boldsymbol{Y}_{\text{acdc}}\boldsymbol{Z}_{\text{net}} \tag{40}$$

Since the impedance of the AC grid only consists of resistance and inductance, it does not contain any right-half plane (RHP) pole. Additionally, it is assumed that both the converter DC- and AC-sides are stable when operating in standalone mode [21]. As a result, Y_{dc} does not contain any RHP pole, and therefore, neither $\boldsymbol{Z}_{\text{net}}$ nor $\boldsymbol{Y}_{\text{acdc}}$ contains any RHP pole. Consequently, the overall system stability can be predicted by analyzing the eigenvalues of the minor loop gain $\boldsymbol{L}$, which is the solution of the following equation:

$$\det(\lambda\boldsymbol{I}_{3\times3} - \boldsymbol{L}) = \det(\lambda\boldsymbol{I}_{3\times3} - \boldsymbol{Y}_{\text{acdc}}\boldsymbol{Z}_{\text{net}}) = 0 \tag{41}$$

Substituting (35) and (37)–(38) into (41) can obtain the eigenvalues. Then, the frequency response of the eigenvalues can be drawn to evaluate the stability of the system. According to the Nyquist criterion, the system is stable when the eigenvalues do not encircle (–1, 0). The main circuit parameters are shown in Table I.

TABLE I
MAIN PARAMETERS OF THE VSC SYSTEM

	Parameters	Value
AC grid	V_g (V)	220
	R_g (Ω)	0.8
	L_g (mH)	5.5
	ω (rad/s)	314
AC filter	L_1 (mH)	3
	C_f (μF)	10
	L_2 (mH)	1
	R_c (Ω)	0.8
DC grid	V_{dc} (V)	700
	C_{dc} (mF)	2
VSC control	P_{VSC} (kW)	5
	f_s (kHz)	10
	T_d (μs)	100
	k_{pdc}	0.3
	k_{idc}	12
	k_{pcc}	2
	k_{icc}	1500
	k_{ppll}	1.387
	k_{ipll}	300

B. Influence of Current Control Loop on VSC System Stability

In order to assess the influence of the positive and negative feedback effects introduced in the CC loop on the VSC system stability, the results are obtained by changing k_{pcc} from 0.5 to 4.6.

Figure 4 shows the frequency responses of the eigenvalues, the grid-tied current waveforms (i_{2abc}), and the DC-link voltage waveforms (v_{dc}) for the VSC system. As shown in Fig. 4(a), the VSC system remains stable with $k_{pcc}=0.5$, as the eigenvalues (λ_1, λ_2, λ_3) do not encircle the point (–1, 0) since the maximum magnitude is –9.9 dB when the phase crosses –180°. Figure 4(b) illustrates the grid-tied current waveform of the VSC at various power levels, with a total harmonic distortion (THD) during full load operation of 1.22%, meeting the grid connection requirements. However, when the VSC output power experiences a sudden variation, the DC voltage waveform exhibits a certain degree of overshoot, with a maximum positive value of 24.1 V.

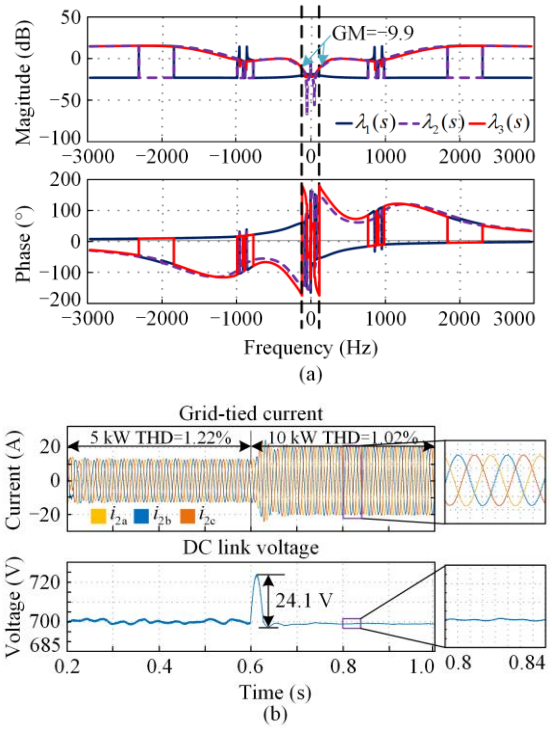
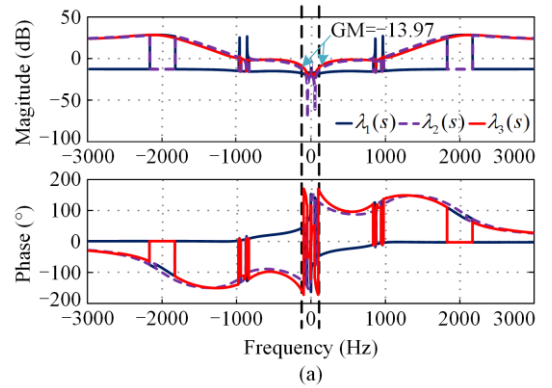


Fig. 4. Stability analysis results of VSC system with $k_{pdc}=0.3$, $k_{pcc}=0.5$. (a) Frequency response of the eigenvalues. (b) Simulated waveforms.

Figure 5(a) plots the frequency responses for $k_{pcc}=2$. The eigenvalues (λ_1, λ_2, λ_3) again do not encircle (–1, 0) since the maximum magnitude is –13.97 dB at the phase crossing of –180°. Thus, compared to $k_{pcc}=0.5$, the stability margin of the VSC is significantly improved, indicating that increasing k_{pcc} from 0.5 to 2 enhances the negative feedback effect, improving the stability of the VSC. It can be seen in Fig. 5(b) that the grid-tied THD is only 0.92% at full load, which is lower than the 1.22% at $k_{pcc}=0.5$. The results are consistent with the frequency domain analysis in Fig. 5(a). However, when there is a sudden change in output power, v_{dc} still exhibits a relatively high overshoot with a peak of 20.2 V, as shown in Fig. 5(b).



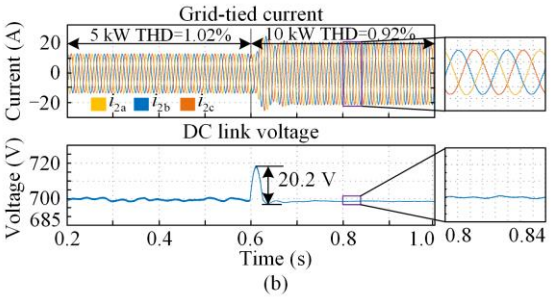


Fig. 5. Stability analysis results of VSC system with $k_{pdc}=0.3$, $k_{pcc}=2$. (a) Frequency response of the eigenvalues. (b) Simulated waveforms.

Similarly, Fig. 6(a) depicts the frequency responses for $k_{pcc}=4.6$, exhibiting a magnitude of 11.2 dB at the phase crossover frequency of 1546 Hz. This observation signifies the system's instability and considerable deviation from the stable boundary. i_{2abc} is presented in Fig. 6(b), demonstrating a significant rise to 32.5% in the THD. Concurrently, v_{dc} waveform exhibits noticeable fluctuations, which matches the resonant frequency analysis in Fig. 6(a). The presented analysis clearly indicates that the increase in k_{pcc} induces a stronger positive feedback effect in the presence of CC influence, diminishing the stability of the system. As a result, the stability of the VSC weakens, ultimately pushing the grid-connected system towards instability. Furthermore, it is worth noting that in addition to the instability observed in $k_{pcc}=4.6$, a significant voltage overshoot of 29.6 V is also observed in v_{dc} when the VSC output power undergoes a sudden change, as shown in Fig. 6(b).

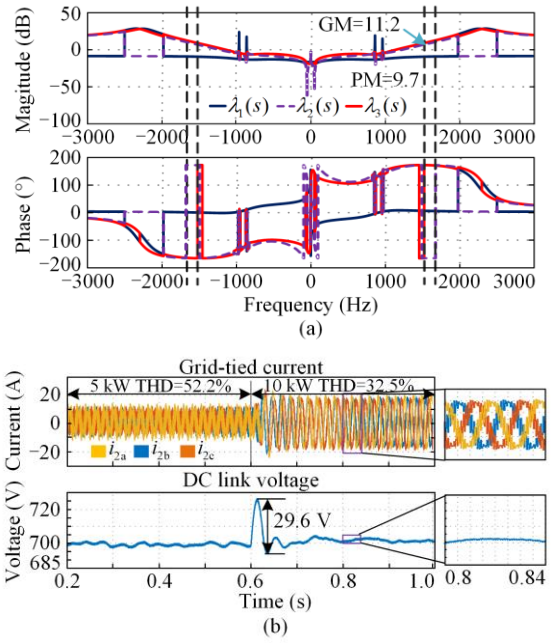


Fig. 6. Stability analysis results of VSC system with $k_{pdc}=0.3$, $k_{pcc}=4.6$. (a) Frequency response of the eigenvalues. (b) Simulated waveforms.

To provide a more visual and effective illustration of the impact of control parameters on the stability of VSC, k_{pcc} is adjusted from 0.1 to 4.6, while the stability of the system is assessed by analyzing the eigenvalues. The stable regions are plotted in Fig. 7, in which the shadowed area indicate stable region according to the eigenvalue analysis, while the line is the boundary. It can be seen that the positive and negative feedback effects generated by the CC parameters within the DVC loop can result in a "turning point" behavior in the stability of VSC. When k_{pcc} increases, the VSC stability exhibits a characteristic of initial enhancement followed by attenuation, as analyzed in the paper. This is different from the characteristic observed in the existing studies [15], [16], which indicate that the stability of weak-grid-tied VSC decreases gradually as the CC loop parameters increase.

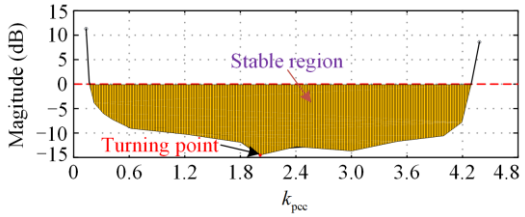


Fig. 7. Stability regions of the VSC system with current loop parameters k_{pcc}.

C. Influence of DC Voltage Control Loop on VSC System Stability

According to the analysis presented in the previous section, modest increase of the parameter k_{pcc} can enhance the stability of the VSC system. However, there are certain levels of overshoots in both the AC current and DC bus voltage during a sudden change in the VSC system output power. Consequently, the overall dynamic response characteristics of the system are negatively affected. Therefore, this section delves further into the impact of the parameters of DVC on the operational features of VSC in weak grid. Stability analysis results are presented for different values of $k_{pdc}=0.01$, 2, and 4.

Figure 8 shows the stability analysis results when $k_{pdc}=0.01$ and $k_{pcc}=2$. Figure 8(a) depicts that the VSC system is stable, because the eigenvalues $(\lambda_1, \lambda_2, \lambda_3)$ do not encircle (−1, 0) since the magnitudes of all eigenvalues are always negative when the phase crosses −180°. However, when the VSC system undergoes a sudden change in output power, significant overshoot can be observed in the grid current and DC bus voltage waveforms, as depicted in Fig. 8(b). Notably, the maximum positive overshoot of the DC bus voltage reaches 14.9 V. Moreover, the time required for the grid current and DC bus voltage to return to steady state is noticeably prolonged.

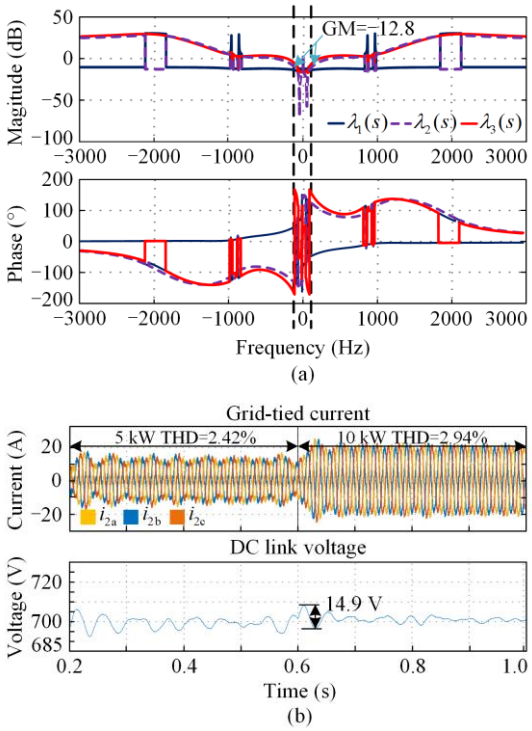
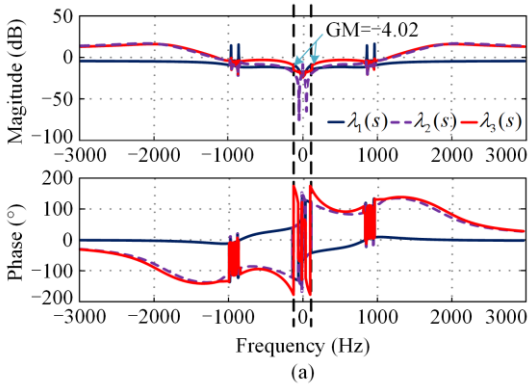


Fig. 8. Stability analysis results of VSC system with $k_{pdc}=0.01$, $k_{pcc}=2$. (a) Frequency response of the eigenvalues. (b) Simulated waveforms.

Figure 9 shows the stability analysis results when $k_{pdc}=2$ while k_{pcc} remains unchanged. Figure 9(a) depicts that the VSC system is stable, because the eigenvalues (λ_1, λ_2, λ_3) do not encircle (−1, 0) either with the magnitudes of the all eigenvalues being negative when the phase crosses −180°. Nevertheless, overshoots are observed in the grid current and v_{dc} waveforms when the VSC system experiences a sudden change in output power, as shown in Fig. 9(b). The maximum positive overshoot of v_{dc} is 12.2 V, and the settling time is about 0.065 s. It is worth noting that increasing the parameters of DVC results in a noteworthy enhancement in the operational performance of the VSC, encompassing both steady-state characteristics and dynamic response, as evidenced by the findings in Figs. 8 and 9.



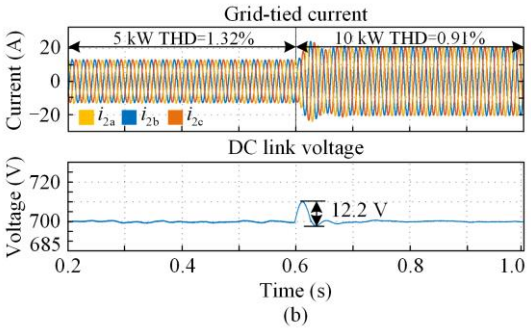


Fig. 9. Stability analysis results of VSC system with $k_{pdc}=2$, $k_{pcc}=2$. (a) Frequency response of the eigenvalues. (b) Simulated waveforms.

Figure 10 illustrates the stability analysis results when k_{pdc} is increased to 4. As seen in Fig. 10(a), the VSC system is stable. When the output power is changed, the maximum positive overshoot of the v_{dc} is reduced to 8.6 V, as shown in Fig. 10(b). However, it takes 0.14 s to recover to the steady-state value of 700 V.

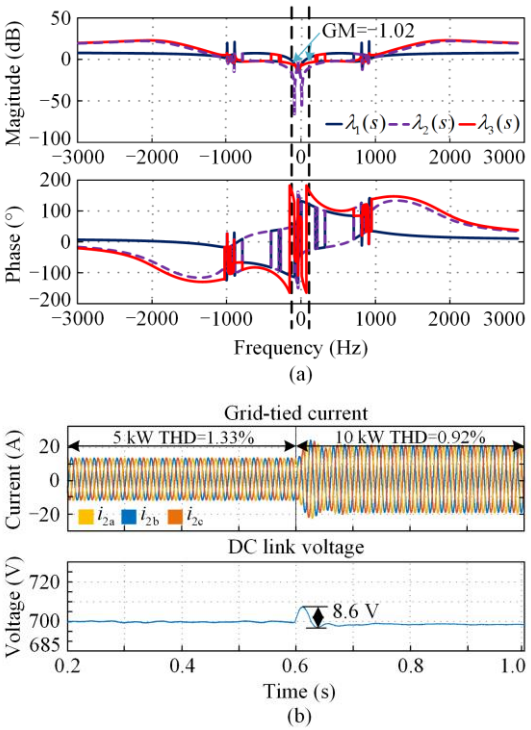


Fig. 10. Stability analysis results of VSC system with $k_{pdc}=4$, $k_{pcc}=2$. (a) Frequency response of the eigenvalues; (b) Simulated waveforms.

Based on the above analysis, compared to adjusting the parameter k_{pdc} of DVC, adjusting the parameter k_{pcc} of CC is more sensitive to stability impact. For example when k_{pdc} varies from 0.01 to 4, the VSC system maintains stable operation, though the dynamic regulation characteristics of the DC bus voltage is impacted significantly. As k_{pdc} increases, the overshoot of the DC

bus voltage gradually reduces from 14.9 V to 8.6 V. The primary reason for this distinction is that the CC introduces positive and negative feedback loops within the entire control structure, significantly affecting the stability of the VSC system. In contrast, the DVC has a minimal impact on the overall system stability, whereas it exhibits a notable influence on the dynamic regulation characteristics of the DC bus voltage.

IV. Experimental Results

In order to further validate the correctness of the above theoretical analysis, a hardware-in-the-loop (HIL) testing setup for the VSC system is constructed, as depicted in Fig. 11. Experimental parameters are consistent with those in Section III.

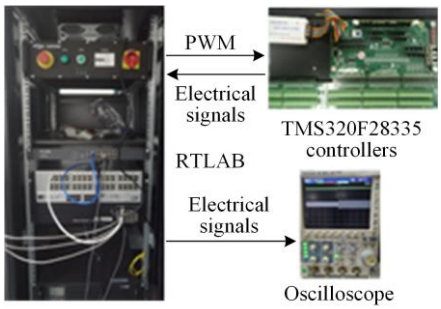


Fig. 11. Hardware-in-the-loop experimental platform.

Case I: To examine the influence of varying the parameter of CC on the system stability, a series of tests are conducted by adjusting k_{pcc} from 0.5 to 4.6.

The observed waveforms of i_{2a} and v_{dc} for the VSC system are presented in Fig. 12. As seen, the system demonstrates stability with $k_{pcc}=0.5$, consistent with the simulation results depicted in Fig. 4. As k_{pcc} is increased to 2, i_{2a} becomes smoother, though when k_{pcc} is further increased to 4.6, i_{2a} exhibits distortion, aligning with the simulation results in Fig. 6(b). Additionally, it can be seen that v_{dc} remain almost unchanged by changing k_{pcc} from 0.5 to 4.6 as shown in Fig. 12, which confirms the agreement between the experimental and simulated outcomes.

Case II: To verify the influence of varying the parameter of DVC on the system stability, tests are conducted by changing k_{pdc} from 0.01 to 4.

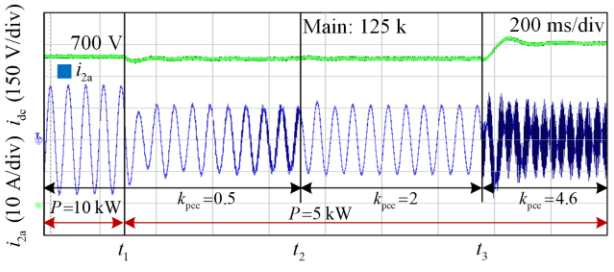


Fig. 12. Experimental results of i_{2a} and v_{dc} with k_{pcc} changes.

Figure 13 depicts the recorded waveforms of i_{2a} and v_{dc} for the VSC system. It can be seen that the voltage and current waveforms are stable when increasing k_{pdc}. Simultaneously, the dynamic regulation characteristics of the DC voltage experience significant enhancement, leading to a gradual reduction in voltage overshoot. These results are consistent with the theoretical analysis presented in Figs. 8–10.

Comparing the experimental results in Fig. 12 and Fig. 13, it shows that the weak-grid-tied interlinking VSC stability is more sensitive to the CC parameter, compared to high impact on the dynamic regulation characteristics by the VDC parameters. The above experimental results verify the correctness of the theoretical analysis in this paper.

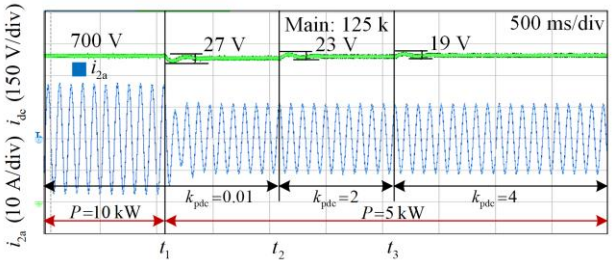


Fig. 13. Experimental results of i_{2a} and v_{dc} with k_{pdc} changes.

V. Conclusion

This paper presents the disparate impact on the stability of the voltage outer loop and current inner loop for weak-grid-tied VSCs. The investigation is conducted using a three-port equivalent small-signal block diagram model. The key features of the paper are outlined below.

1) Taking into account the AC- and DC-side dynamics under weak grid, the current inner loop controller exhibits positive and negative feedback effects within the DC-link voltage outer loop. The influence of this interaction on the stability is characterized by a dual role.

2) The introduced positive and negative feedback effects result in a distinctive "turning point" behavior in the VSC stability. Consequently, when the parameters of the current loop controller are increased, the system's stability undergoes an initial improvement, followed by subsequent attenuation.

3) The sensitivity of the system's stability is higher to variations in the parameters of the current control loop, whereas the dynamic regulation characteristic is more sensitive to changes in the parameters of the voltage control loop.

It is worth noting that further exploration is needed in the future to seek the critical point where positive and negative feedback effects cancel each other by constructing mathematical analytic expressions or quantitative indicators.

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AUTHORS' CONTRIBUTIONS

Zhiwei Zeng: original draft preparation, conceptualization, methodology, experimental, and formal analysis. Jinbin Zhao: supervision, reviewing, and editing. Sujie Zhang: simulation, reviewing, and editing. Ling Mao: conceptualization, methodology, and original draft preparation. Keqing Qu: supervision, reviewing, editing, and validation. All authors read and approved the final manuscript.

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AVAILABILITY OF DATA AND MATERIALS

Not applicable.

DECLARATIONS

Competing interests: The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this article.

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